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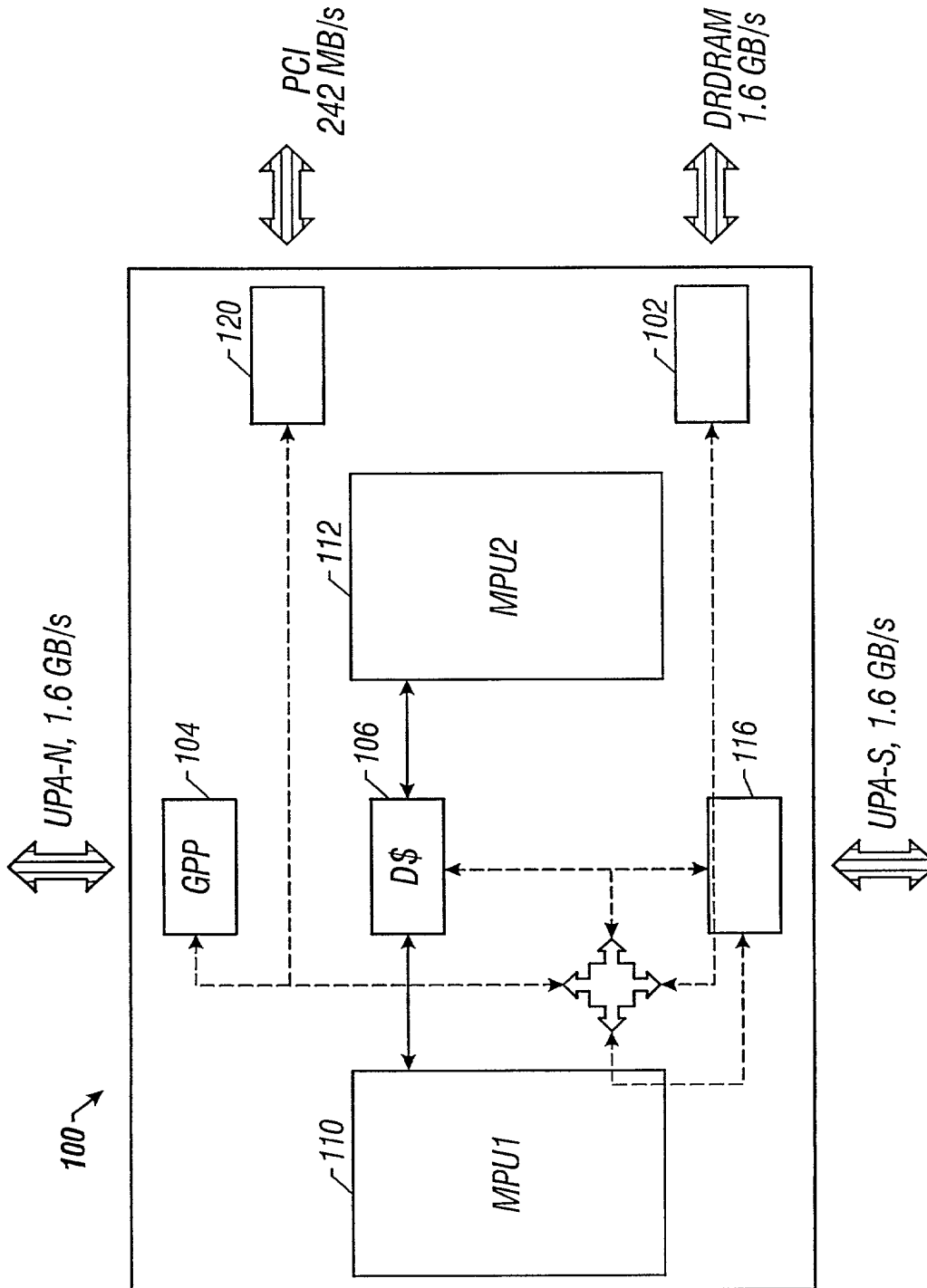


FIG. 1

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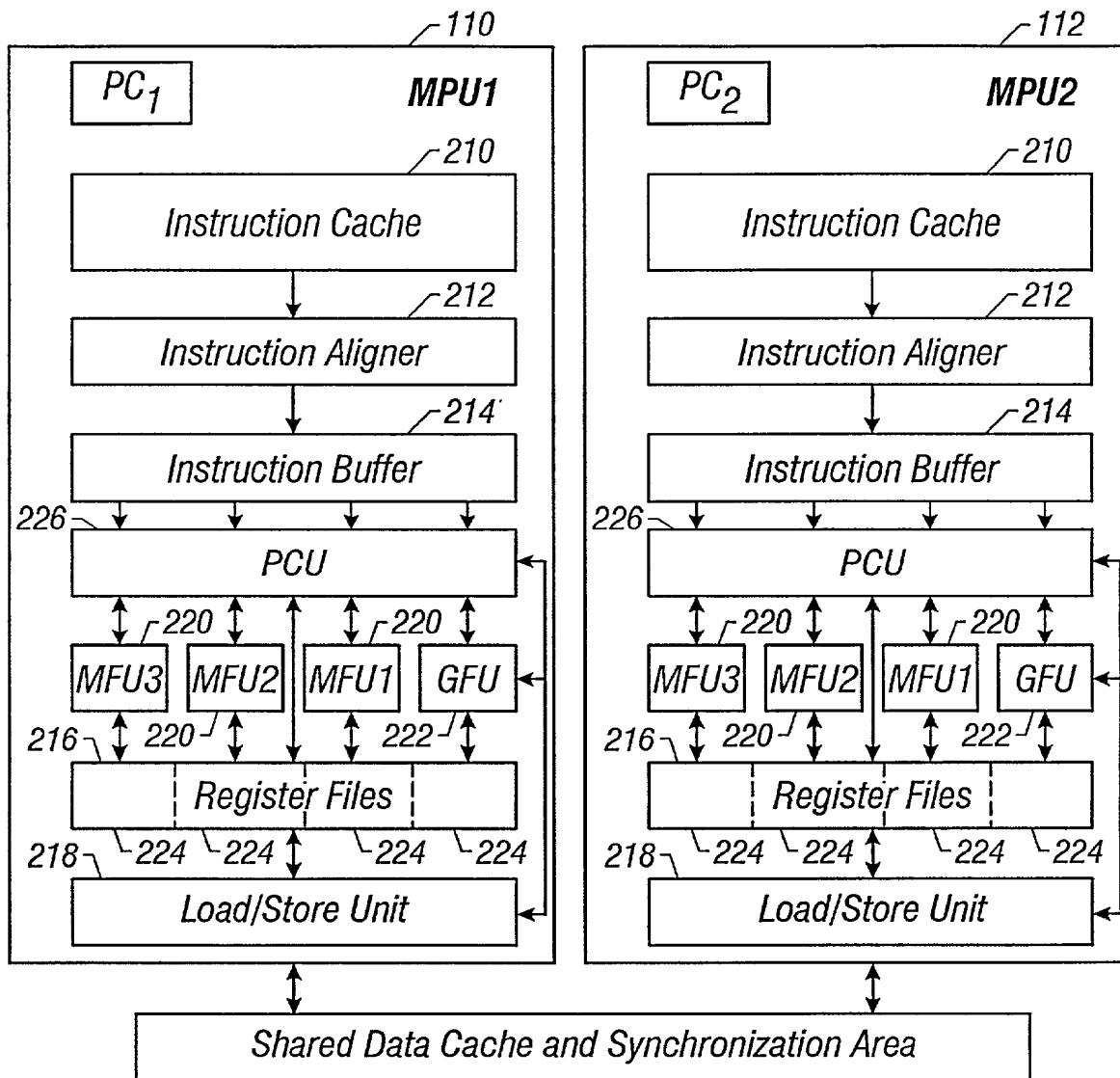


FIG. 2

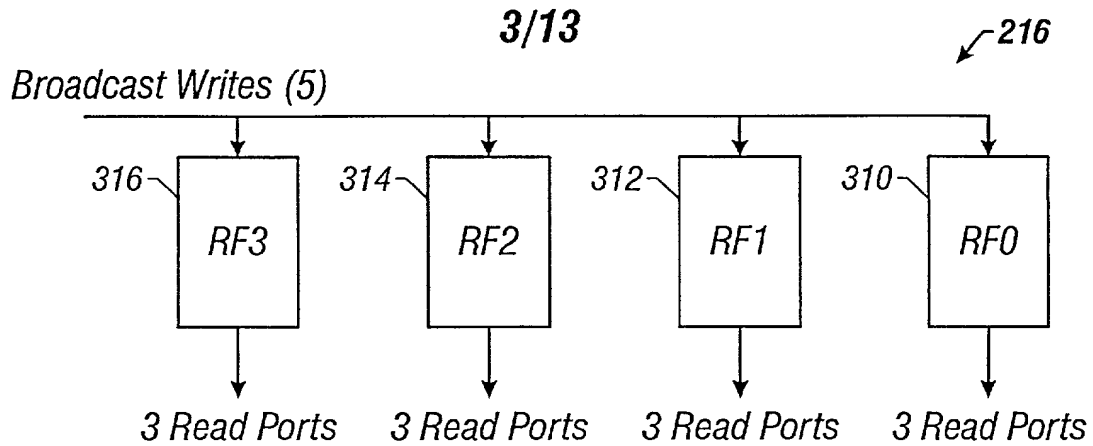


FIG. 3

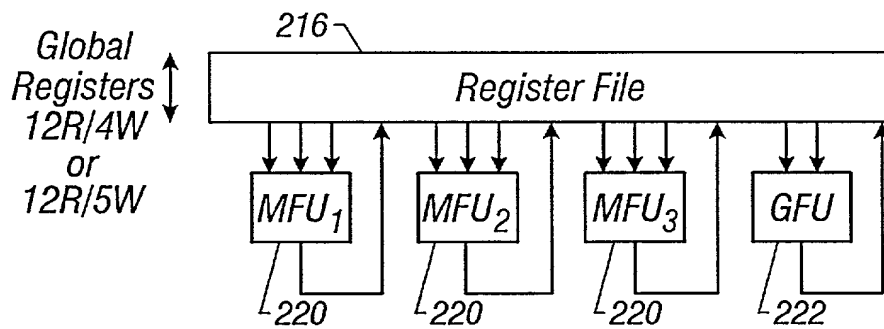


FIG. 4

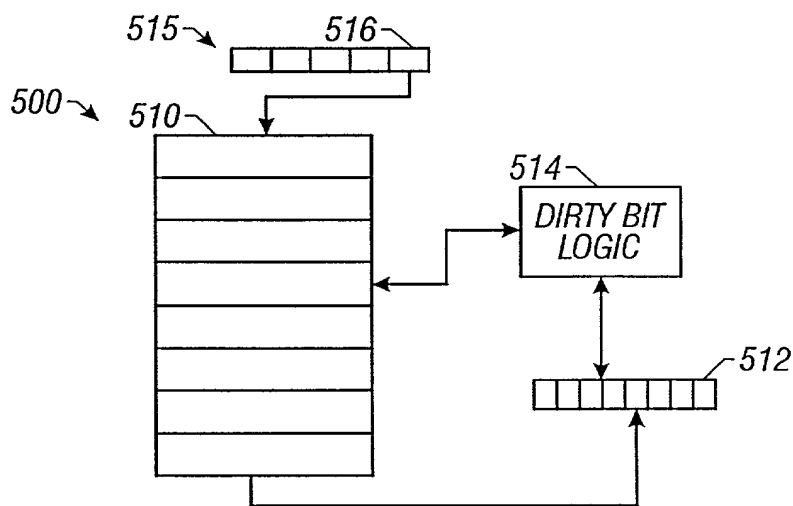


FIG. 5

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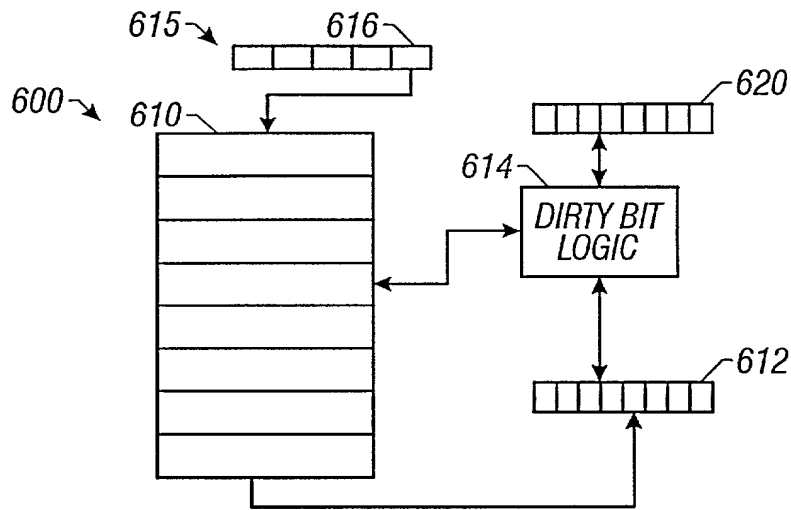


FIG. 6

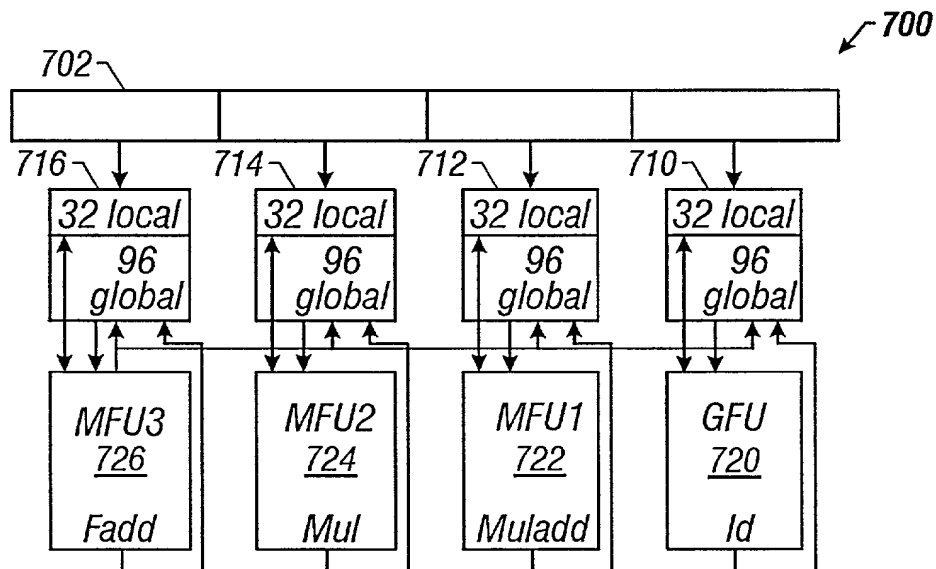


FIG. 7

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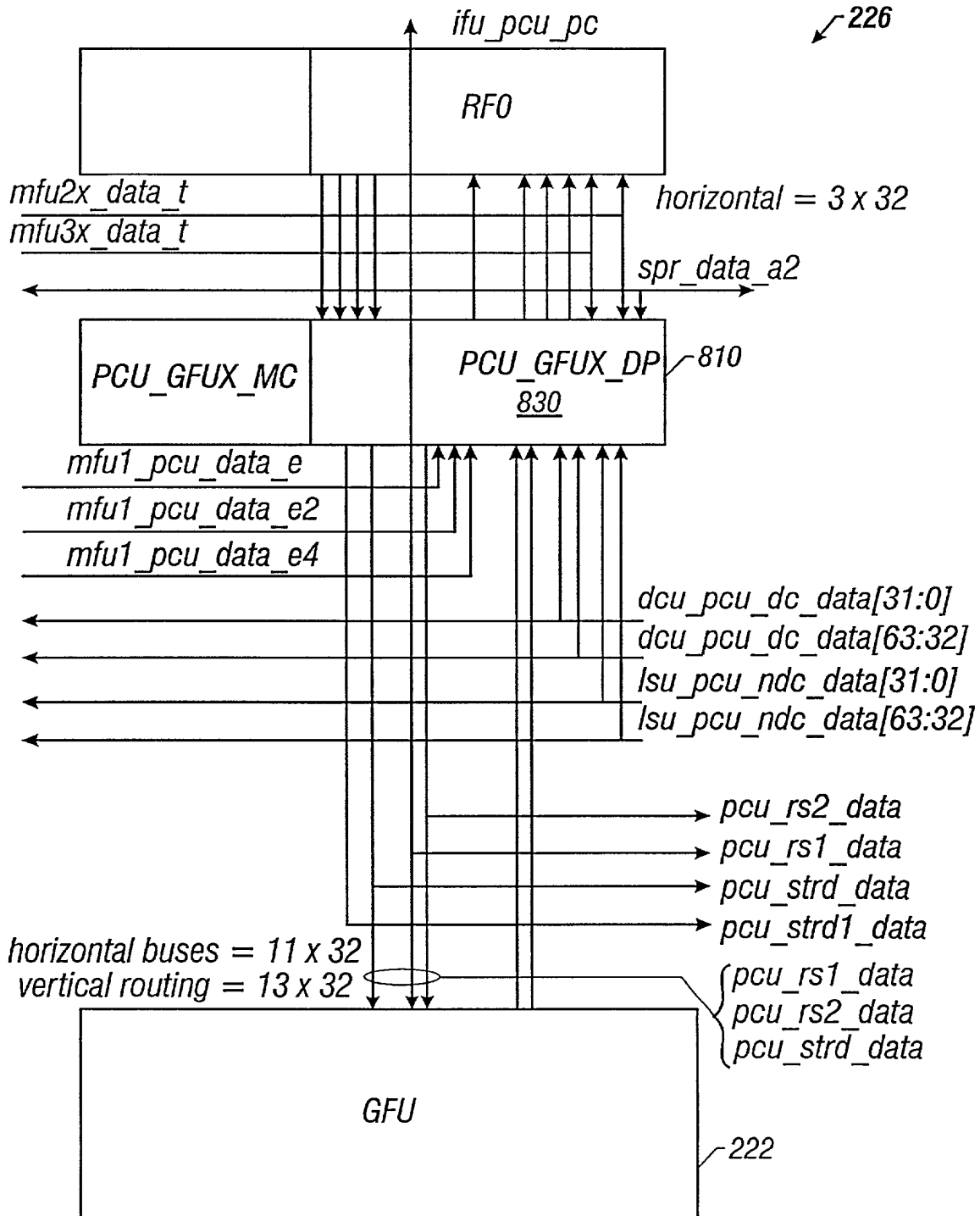


FIG. 8A

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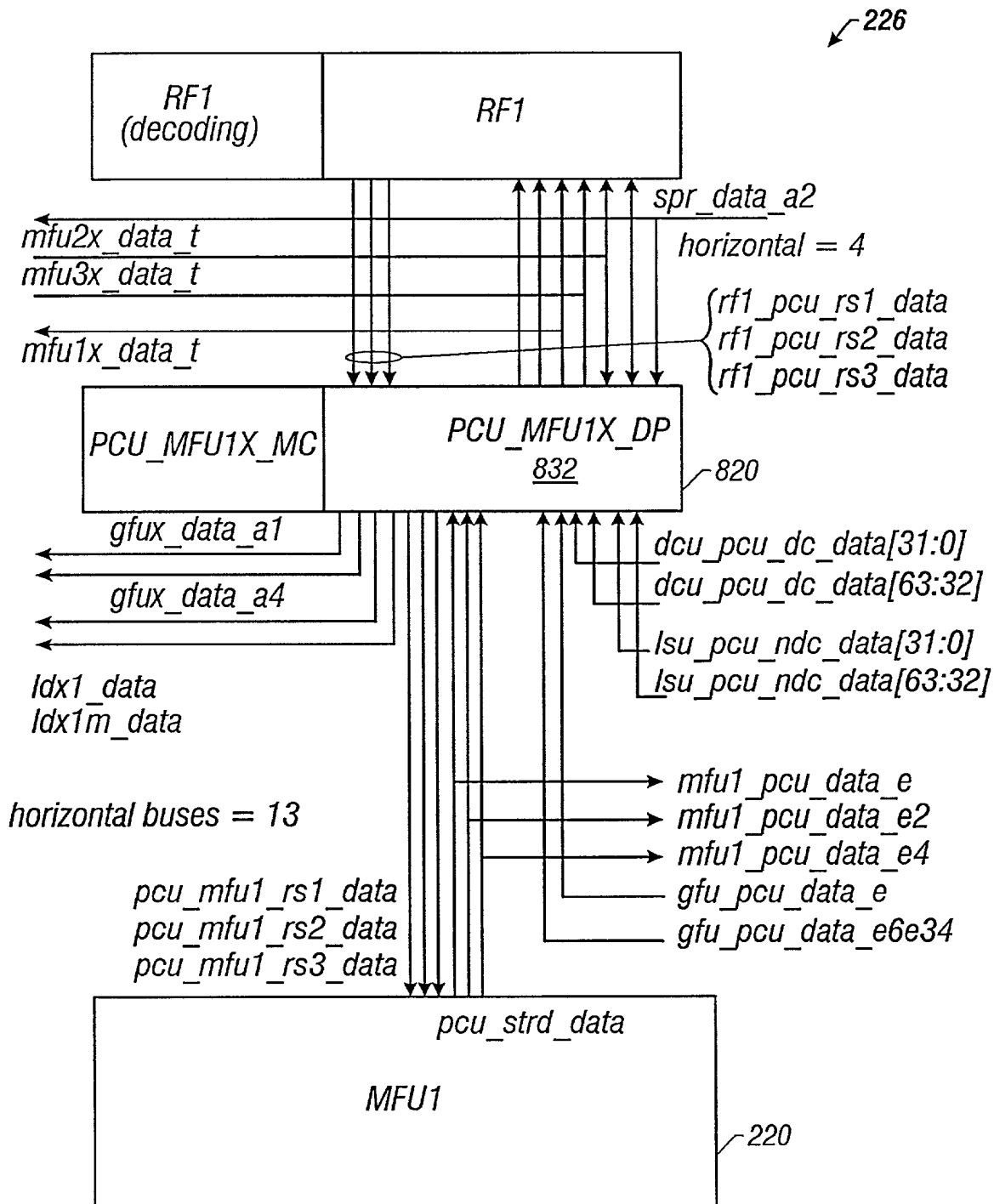


FIG. 8B

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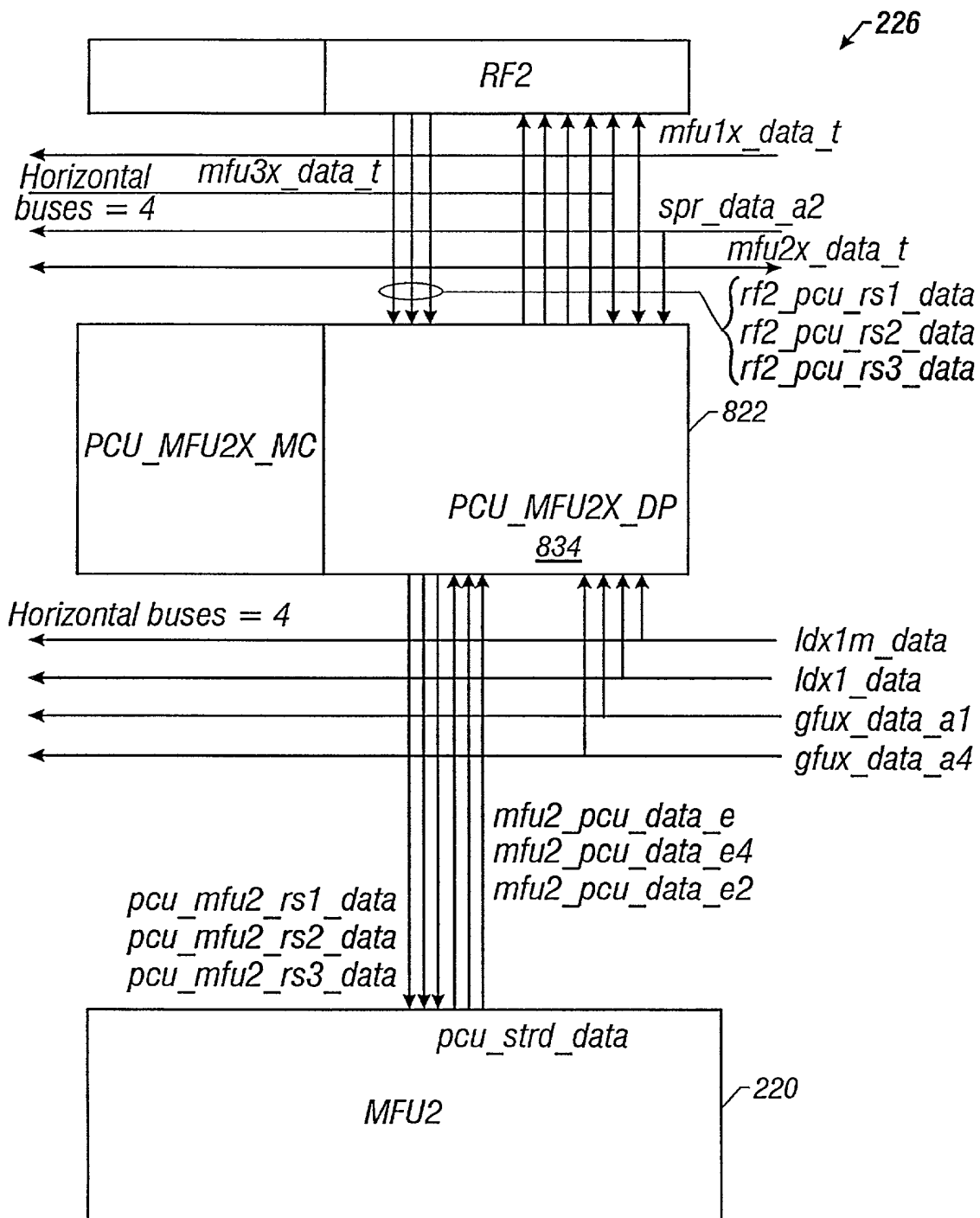


FIG. 8C

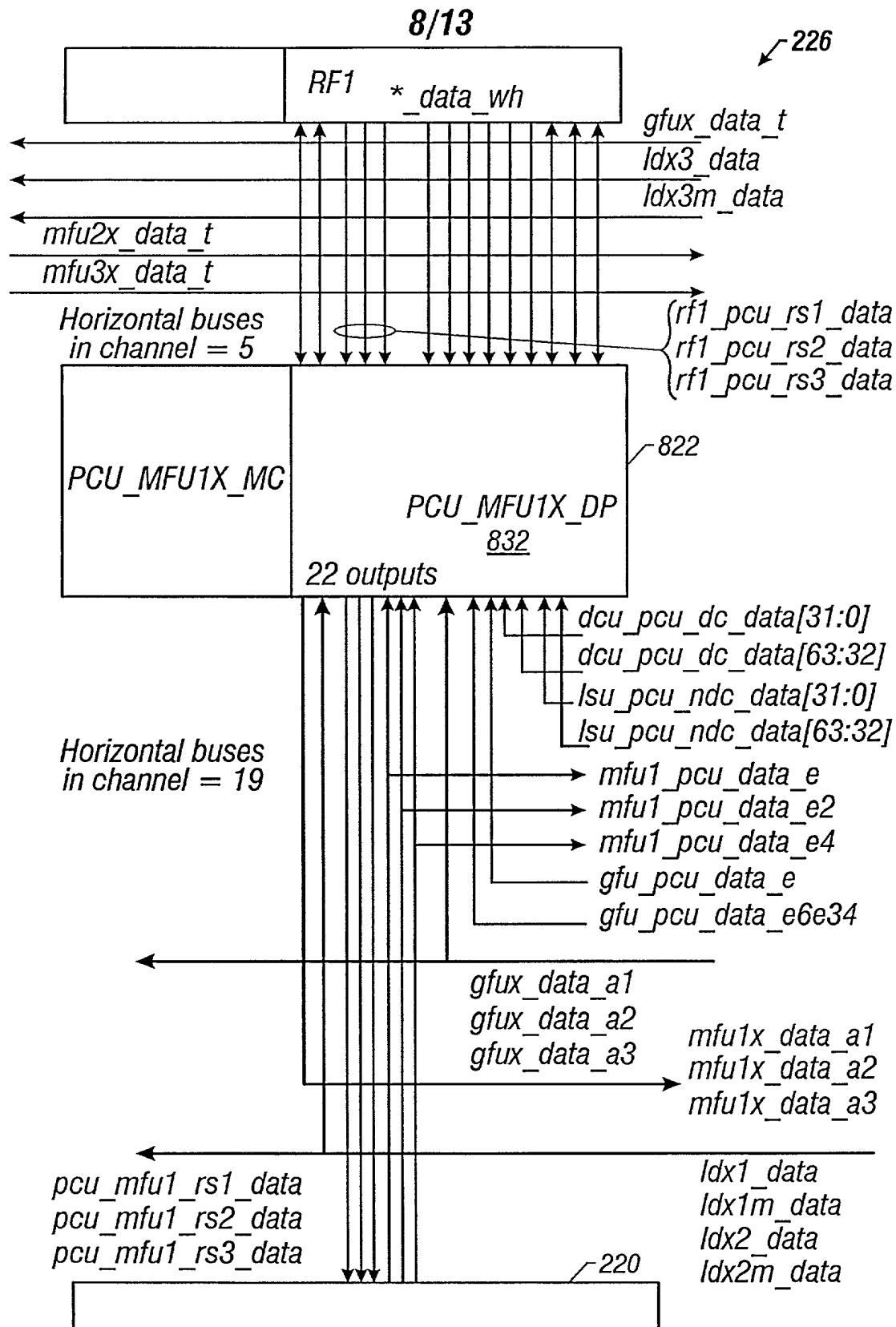


FIG. 8D

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<i>Register name</i>	<i>width</i>	<i>address specifier</i>	<i>user access</i>	<i>supervisor access</i>	<i>thread state</i>
<i>PSR</i>	8	010_0001	no	rd/wr	yes
<i>TPSR1</i>	8	010_0010	no	"	yes
<i>TPSR2</i>	8	010_0011	no	"	yes
<i>PCR</i>	7	010_0000	no	"	no
<i>TL</i>	2	010_0100	no	"	no
<i>TICK</i>	32	010_0101	read only	"	no
<i>TVALUE</i>	32	010_0110	no	"	no
<i>TCNTL</i>	8	010_0111	no	"	no
<i>GX</i>	13	001_0000	no	rd only	yes
<i>INT</i>	7	010_1000	no	rd/wr	yes
<i>FSR</i>	16	001_0001	rd/wr	"	yes
<i>FMT</i>	2	010_1010	rd/wr	rd/wr	yes
<i>DIRTY</i>	6	010_1011	rd/wr	"	yes
<i>INT_OTHER</i>	—	010_1001	no	wr only	yes

FIG. 9

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<i>PCR</i>	<i>PCR</i>	<i>Description</i>	<i>Initial value</i>	<i>After a trap</i>
[0]	POW	power management	0 (off)	N/C not changed
[1]	ICE	icache enable	0	"
[2]	DCE	dcache enable	0	"
[3]	BPTE	branch predict taken enable	0	"
[4]	PE	pipeline enable	0	"
[5]	MSTEP	memory step	0	"
[6]	PID	processor ID	hardwired	hardwired

FIG. 10

<i>Instruction</i> <i>vliw_1</i>	<i>Instruction</i> <i>setir ra, PSR</i>
<i>vliw_2</i>	<i>ld_2 [r1+r2], r3</i>
<i>vliw_3</i>	<i>ld_3</i>
<i>vliw_4</i>	<i>ld_4</i>
<i>vliw_5</i>	<i>ld_5</i>
<i>vliw_6</i>	<i>ld_6</i>

FIG. 11A

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cycle	1	2	3	4	5	6	7	8	9	10	11	12
setir	D	E	A1	A2	A3	T	WB					
ld_2		D	E	A1	A2	A3	T	WB				
ld_6						D	E	E				
ld_7												

1114

1150

1124

1122

FIG. 11B

Instruction	Instruction
vliw_1	setir ra, PCR
vliw_2	inst 2
vliw_3	inst 3
vliw_4	inst 4
vliw_5	inst 5
vliw_6	inst 6
vliw_7	inst 7
vliw_8	inst 8
vliw_9	setir rb, PSR
vliw_10	inst 10
vliw_11	inst 11

FIG. 12A

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	1212				1222								
cycle	1	2	3	4	5	6	7	8	9	10	11	12	13
setir	T	WB											
inst7		D	D	E	A1	A2	A3	T	WB				
inst8				D	D	D	D	D	D	D	E	A1	A2
setir											D	D	D
iST		ST		ST	ST	ST	ST	ST	ST		ST	ST	ST

	1254												
cycle	14	15	16	17	18	19	20	21	22	23	24	25	26
inst8	A3	T	WB										
setir	D	D	D	D	E	A1	A2	A3	T	WB			
inst10					D	D	D	D	D	D	E	A1	A2
inst11											D	E	A1
ST	ST	ST	ST		ST	ST	ST	ST	ST				

FIG. 12B

1300

Instruction	Unit	rd [6:5]
[0]	all	01
[1]	all	10
[2]	gfu	11
[3]	mfu1	11
[4]	mfu2	11
[5]	mfu3	11

FIG. 13

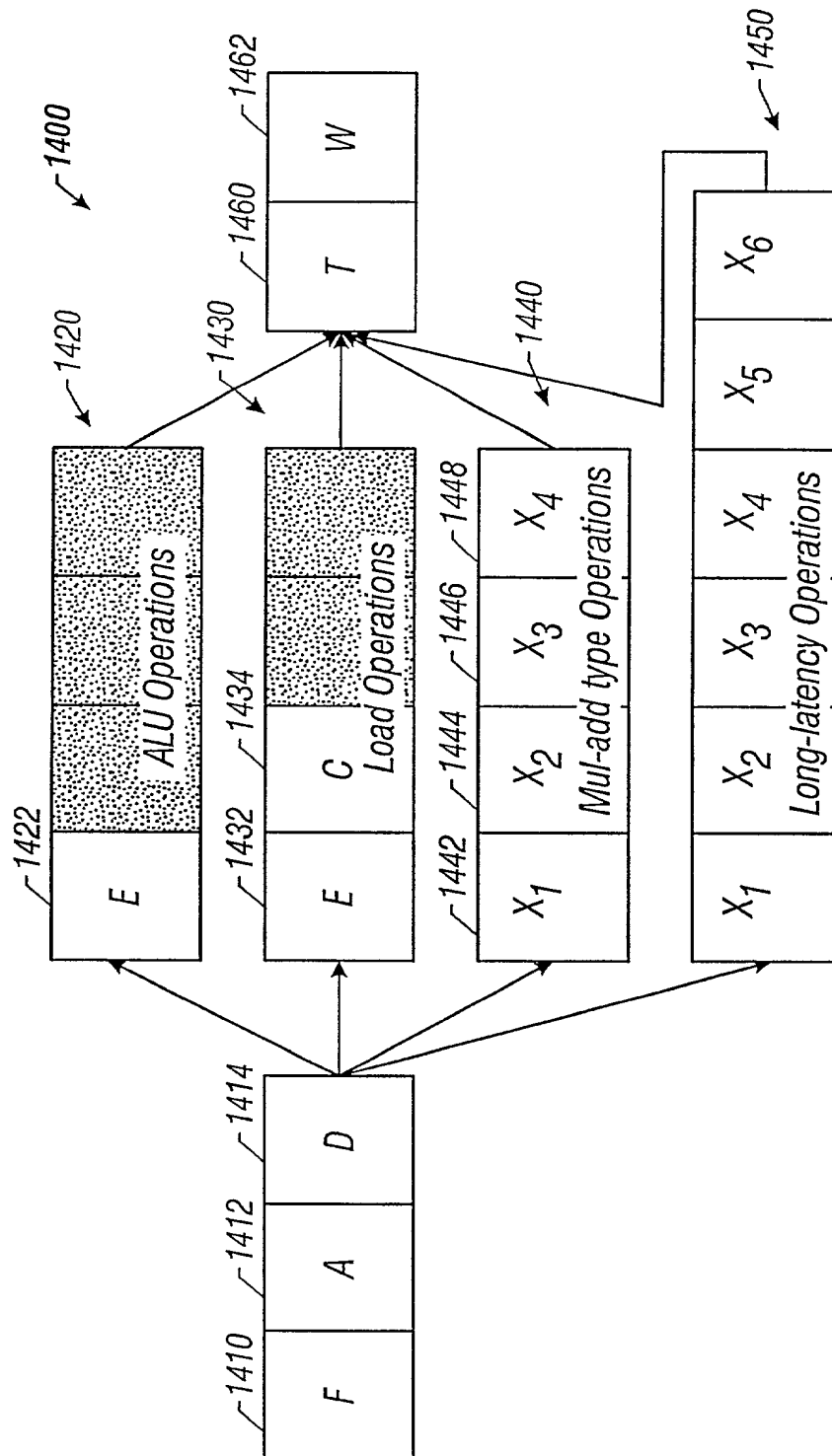


FIG. 14